UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,793	05/14/2002	Kuo-Tso Chen	8192-US-PA	1583

31561 7590 02/25/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,793	CHEN ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: ACCURATUS data sheets for Alumina (4 sheets) and Aluminum Nitride (2 sheets).

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed November 24, 2004. The Examiner acknowledges the amendments to Claims 1, 6, 8, 13, 15, 21, 23 and 29. Accordingly, Claims 1-30 remain pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejection hereinbelow:

Wachtler et al. (US 6,274,391 B1)† Cheng et al. (US 2003/0134455 A1)†

Viswanathan et al. (US 6,724,079 B2)

Accuratus data sheets on the properties of alumina and aluminum nitride.

†Already of record in the instant Application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 3-8, 10-15, 18-25 and 28-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Wachtler et al. in view of Viswanathan et al.

A) As to Claims 1 and 8:

I. Wachtler et al. discloses: a substrate 12 having a first surface (Fig. 8; bottom surface of cavity 14); a chip 16 having an active surface with a plurality of bonding pads thereon (col.8: 63-67) and a backside surface attached to the first surface of substrate 12 (Fig. 9); and a build-up circuit structure 18 on substrate 12 (Fig. 22), the build-up structure having at least one insulation layer 24 and 26 (Figs. 10-12; col.9: 1-18), at least one patterned circuit layer 34 and a plurality of via openings 28 and 40 (col.9: 19-40; Figs. 14-22), wherein the at least one insulation layer 24 and 26 is located between the active surface and the patterned circuit layer 34 (Fig. 14), the via openings 28 corresponding to the bonding pads pass through the at least one insulation layer 24 and 26 (Fig. 12; col.9: 19-23), wherein the via openings 28 are deposited with a conductive material 30, the at least one patterned circuit layer 34 electrically connects with the bonding pads through the conductive material 30 (which, after patterning, form the via filling material 32 as well as the circuit layer 34) [col.9: 19-40] and a portion of the at least one patterned circuit layer 34 expands into a region outside the active surface of the chip (Figs. 14 and 22 show only one portion of the patterned circuit layer 34

expanded to a region outside the active surface of the chip, Figs. 7 and 26 show the inherent expansion of the *entirety* of the at least one patterned circuit layer 34 throughout the high density interconnect overlay 18, including a region outside the active surface of the chip, and col.9: 32-40).

II. Wachtler et al. further discloses, in the embodiment of Fig. 31, that substrate 12 comprises a conductive path 58 (i.e., a conductive through-hole) built through the substrate to allow an alternative electrical path off the back side of the substrate in order to establish connections to other electronic devices, such as a printed wiring board (col.12: 24-38). Wachtler et al. does not teach that substrate 12 comprises an internal circuit.

III. Viswanathan et al. discloses a semiconductor IC device 130 (col.3: 20-25) electrically connected through a multilayered interconnect system 124 (col.3: 39-43) to a substrate 140 comprising an internal circuit 141 that provides noise suppression, signal conditioning or impedance matching for the purpose of improving the performance of the semiconductor IC device 130 (col.4: 49-col.5: 18).

IV. Since both Wachtler et al. and Viswanathan et al. are both practitioners in the same art of packaging semiconductor devices to circuit substrates, and Wachtler et al. teaches a conductive through-hole built through the circuit substrate for creating an electrical path between the build-up circuit structure and circuitry on the back side of the substrate for establishing external connections, then the further modification of the substrate to include a more extensive internal circuit for providing filtering or impedance control, as taught by Viswanathan et al., would have been readily recognized as a

further enhancement to the performance of the chip package in the pertinent art of Wachtler et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the through-hole substrate of the semiconductor chip package of Wachtler et al. by including therein the internal circuit taught by Viswanathan et al. in order to provide in the semiconductor package of Wachtler et al. at least one of noise suppression, signal conditioning or impedance matching for improving the performance of the semiconductor chip device, as taught by Viswanathan et al.

B) As to Claims 3, 10 and 11, modified Wachtler et al. further discloses: a plurality of solder ball pads 44 on the at least one patterned circuit layer 34 (Figs. 19 and 20); and a plurality of solder balls 22 attached to the solder ball pads, respectively (Fig. 21) [col.10: 26-27].

C) As to Claim 4, modified Wachtler et al. further discloses a passivation layer 46 disposed on the at least one patterned circuit layer 34, wherein the passivation layer 46 has a plurality of openings corresponding to solder ball pads 44 (Fig. 21; col.10: 23-26).

D) As to Claims 5 and 12, modified Wachtler et al. further discloses that substrate 12 is a plastic (i.e., polymer) material (col.8: 37-43).

E) As to Claims 6, 7, 13 and 14:

I. Wachtler et al., as modified by Viswanathan et al. discloses that the substrate comprises an internal circuit that provides noise suppression, signal conditioning or impedance matching for the purpose of improving the performance of the

semiconductor IC device (see col.4: 49-col.5: 18 in Viswanathan et al.). It remains to be shown that Wachtler et al. in view of Viswanathan et al. also discloses that the internal circuit in the substrate comprises at least one of a capacitor and an inductor (Claims 6 and 13) and that the internal circuit and the bonding pads on the chip are electrically connected (Claims 7 and 14).

II. Viswanathan et al. further discloses that, in order to provide the above-cited circuit enhancements, the internal circuit 141 comprises at least one of a capacitor and an inductor (col.4: 49-57) and is electrically connected to the bonding pads on the chip (the bonding pads 124 of semiconductor chip 130 are electrically connected to the internal circuit 141; see Figs. 1 and 3, and col.3: 20-25 and 39-46).

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the internal circuit of Wachtler et al., as modified by Viswanathan et al., with the inclusion of at least one of a capacitor and an inductor in order to perform the particular noise suppression, signal conditioning or impedance matching circuit(s) required by the specific electronic application of the package, with the internal circuit being electrically connected to the chip bonding pads in order for the internal circuit of the substrate to perform the above-cited filtering and impedance operations for enhancing the performance of the chip and, thereby, the semiconductor package, as taught by Viswanathan et al.

F) As to Claims 15 and 23:

I. Wachtler et al. discloses: a substrate 12 having a first surface and at least one cavity 14 located on the first surface of the substrate (Fig. 8); a chip 16 having an active

surface with a plurality of bonding pads thereon (col.8: 63-67) and a backside surface attached to the bottom of cavity 14 (Fig. 9); and a build-up circuit structure on substrate 12 (Fig. 22), the build-up structure having at least one insulation layer 24 and 26 (Figs. 10-12; col.9: 1-18), at least one patterned circuit layer 34 and a plurality of via openings 28 and 40 (col.9: 19-40; Figs. 14-22), wherein the at least one insulation layer 24 and 26 is located between the active surface and the patterned circuit layer 34 (Fig. 14), the via openings 28 corresponding to the bonding pads pass through the at least one insulation layer 24 and 26 (Fig. 12; col.9: 19-23), wherein the via openings 28 are deposited with a conductive material 30, the at least one patterned circuit layer 34 electrically connects with the bonding pads through the conductive material 30 (which, after patterning, form the via filling material 32 as well as the circuit layer 34) [col.9: 19-40] and a portion of the at least one patterned circuit layer 34 expands into a region outside the active surface of the chip (Figs. 14 and 22 show only one portion of the patterned circuit layer 34 expanded to a region outside the active surface of the chip, Figs. 7 and 26 show the inherent expansion of the *entirety* of the at least one patterned circuit layer 34 throughout the high density interconnect overlay 18, including a region outside the active surface of the chip, and col.9: 32-40).

II. Wachtler et al. further discloses, in the embodiment of Fig. 31, that substrate 12 comprises a conductive path 58 (i.e., a conductive through-hole) built through the substrate to allow an alternative electrical path off the back side of the substrate in order to establish connections to other electronic devices, such as a printed wiring board

(col.12: 24-38). Wachtler et al. does not teach that substrate 12 comprises an internal circuit.

III. Viswanathan et al. discloses a semiconductor IC device 130 (col.3: 20-25) electrically connected through a multilayered interconnect system 124 (col.3: 39-43) to a substrate 140 comprising an internal circuit 141 that provides noise suppression, signal conditioning or impedance matching for the purpose of improving the performance of the semiconductor IC device 130 (col.4: 49-col.5: 18).

IV. Since both Wachtler et al. and Viswanathan et al. are both practitioners in the same art of packaging semiconductor devices to circuit substrates, and Wachtler et al. teaches a conductive through-hole built through the circuit substrate for creating an electrical path between the build-up circuit structure and circuitry on the back side of the substrate for establishing external connections, then the further modification of the substrate to include a more extensive internal circuit for providing filtering or impedance control, as taught by Viswanathan et al., would have been readily recognized as a further enhancement to the performance of the chip package in the pertinent art of Wachtler et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the through-hole substrate of the semiconductor chip package of Wachtler et al. by including therein the internal circuit taught by Viswanathan et al. in order to provide in the semiconductor package of Wachtler et al. at least one of noise suppression, signal conditioning or impedance matching for

improving the performance of the semiconductor chip device, as taught by Viswanathan et al.

G) As to Claims 18, 24 and 25, modified Wachtler et al. further discloses: a plurality of solder ball pads 44 on the at least one patterned circuit layer 34 (Figs. 19 and 20); and a plurality of solder balls 22 attached to the solder ball pads, respectively (Fig. 21) [col.10: 26-27].

H) As to Claim 19, modified Wachtler et al. further discloses a passivation layer 46 disposed on the at least one patterned circuit layer 34, wherein the passivation layer 46 has a plurality of openings corresponding to solder ball pads 44 (Fig. 21; col.10: 23-26).

I) As to Claims 20 and 28, modified Wachtler et al. further discloses that substrate 12 is a plastic (i.e., polymer) material (col.8: 37-43).

J) As to Claims 21, 22, 29 and 30:

I. Wachtler et al., as modified by Viswanathan et al. discloses that the substrate comprises an internal circuit that provides noise suppression, signal conditioning or impedance matching for the purpose of improving the performance of the semiconductor IC device (see col.4: 49-col.5: 18 in Viswanathan et al.). It remains to be shown that Wachtler et al. in view of Viswanathan et al. also discloses that the internal circuit in the substrate comprises at least one of a capacitor and an inductor (Claims 21 and 29) and that the internal circuit and the bonding pads on the chip are electrically connected (Claims 22 and 30).

II. Viswanathan et al. further discloses that, in order to provide the above-cited circuit enhancements, the internal circuit 141 comprises at least one of a capacitor and an inductor (col.4: 49-57) and is electrically connected to the bonding pads on the chip (the bonding pads 124 of semiconductor chip 130 are electrically connected to the internal circuit 141; see Figs. 1 and 3, and col.3: 20-25 and 39-46).

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the internal circuit of Wachtler et al., as modified by Viswanathan et al., with the inclusion of at least one of a capacitor and an inductor in order to form the particular noise suppression, signal conditioning or impedance matching circuit(s) required by the specific electronic application of the package, with the internal circuit being electrically connected to the chip bonding pads in order for the internal circuit of the substrate to perform the above-cited filtering and impedance operations for enhancing the performance of the chip and, thereby, the semiconductor package, as taught by Viswanathan et al.

6. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Wachtler et al. and Viswanathan et al., in conjunction with the *Accuratus* data sheets on alumina and aluminum nitride.

A) As to Claims 1 and 8:

I. Cheng et al. discloses: a substrate 300 having a first surface (the bottom of cavity 306; Fig. 15); a chip 310 having an active surface 310a with a plurality of bonding pads 312 thereon and a backside surface 310b attached to the first surface of the substrate (p.3, paragraph [0033]); and a build-up circuit structure on substrate 300 (Fig.

23; p.3: paragraphs [0033]-[0042]), the build-up circuit structure having at least one insulation layer 314a (Fig. 17; paragraph [0034]), at least one patterned circuit layer 320a (Fig. 19; p.3, paragraph [0037]) and a plurality of via openings 316 (Fig. 17), wherein the insulation layer 314a is located between the active surface 310a and the at least one patterned circuit layer 320a (Fig. 19), the via openings 316 corresponding to bonding pads 312 pass through the insulation layer (Fig. 17) {p.3, paragraph [0034]}, wherein the via openings 316 are deposited with a conductive material 320 (Fig. 18; p.3: paragraph [0037]), the at least one patterned circuit layer 320a electrically connects with the bonding pads 312 through the conductive material 320 and a portion of the at least one patterned circuit layer 320a expands into a region outside the active surface of the chip (Fig. 19).

II. Cheng et al. discloses that substrate 300 comprises the combination of a metallic plate 301 and thermally conductive--metal or non-metal--plate 308 (Figs. 14 and 24, and 25-27; p.3, paragraphs [0041] and [0042]), said substrate 300 thereby functioning as a heat dissipation structure for channeling heat away from the packaged semiconductor device chip 310 in Fig. 24 (p.3, last four lines of paragraph [0042]).

III. Wachtler et al. discloses, in Figs. 7, 8 and 31, a substrate 12 for mounting and packaging a chip 16 that functions as a part of the circuit package (Figs. 22 and 31), having a conductive through-hole passage 58 for enabling an electrical path on the back side of the substrate 12 for external connection to other devices (col.12: 24-38), and is made of a thermally conductive material (e.g., ceramic, aluminum nitride; see also Sheet 1 of each of the *Accuratus* data sheets for alumina and aluminum nitride) for

channeling heat away from the chip 16 (col.8: 37-46). Consequently, Wachtler et al. teaches a substrate 12 that functions as both an interconnection circuit and a heat dissipation device.

IV. Viswanathan et al. discloses a semiconductor IC device 130 (col.3: 20-25) electrically connected through a multilayered interconnect system 124 (col.3: 39-43) to a substrate 140 comprising an internal circuit 141 that provides noise suppression, signal conditioning or impedance matching for the purpose of improving the performance of the semiconductor IC device 130 (col.4: 49-col.5: 18). Viswanathan et al. further discloses that the substrate 140 is made of any of a number of materials, depending on the electronic application of the package, including alumina and aluminum nitride (col.4: 10-26) which are known good thermally conducting materials (see Sheet 1 of *Accuratus* data sheet on Aluminum Oxide--i.e., Alumina--and Sheet 1 of *Accuratus* data sheet on Aluminum Nitride under the Key Properties section).

V. Since Cheng et al., Wachtler et al. and Viswanathan et al. are all in the same art of semiconductor device packaging, and both Cheng et al. and Wachtler et al. disclose similar packages that require a heat dissipating substrate, the substrate of Wachtler et al. formed of a ceramic material or aluminum nitride and further functioning as an interconnect substrate comprising at least one conductive through-hole, and Viswanathan et al. teaches a substrate made of any material required by the package application, including alumina and aluminum nitride which have good thermally conductive properties (as taught in the above-mentioned *Accuratus* data sheets), said substrate of Viswanathan et al. further comprising an internal circuit for enhancing the

performance and reliability of the packaged semiconductor device, then the modification of the heat dissipation substrate of Cheng et al. with the heat dissipating circuit substrate of Wachtler et al., the circuit modification of Cheng et al. by Wachtler et al. being further enhanced by the internal circuit structure of the thermally conductive substrate in Viswanathan et al. for providing signal conditioning and impedance control in the semiconductor package, would have been readily recognized as valuable enhancements to the performance and reliability of the semiconductor package in the pertinent art of Cheng et al.

VI. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the heat dissipating substrate of Cheng et al. with the heat dissipating circuit substrates of Wachtler et al. and Viswanathan et al., for enhancing the performance and reliability of the semiconductor package in Cheng et al., and further modifying the substrate Cheng et al. with the internal circuit of the substrate of Viswanathan et al. in order to provide noise suppression, signal conditioning or impedance matching for the purpose of improving the performance and reliability of the semiconductor package of Cheng et al., as taught by Viswanathan et al.

B) As to Claims 2 and 9, modified Cheng et al. further discloses the space, in cavity 306, between chip 310 and substrate 300 is filled by the material of insulation layer 314a (Figs. 16 and 17; p.3, lines 1-4 of paragraph [0034] and lines 1-5 of paragraph [0035]).

C) As to Claims 3, 10 and 11, modified Cheng et al. further discloses a plurality of solder ball pads on the at least one patterned circuit layer 326a, and a plurality of

solder balls 330 attached to the solder ball pads, respectively (Fig. 24; p.3, paragraph [0040]).

D) As to Claim 4, modified Cheng et al. further discloses a passivation layer 328 disposed on the patterned circuit layer 326a, wherein passivation layer 328 has a plurality of openings 329 corresponding to the solder ball pads (Figs. 23 and 24; paragraph [0039]).

E) As to Claims 5 and 12, modified Cheng et al. further discloses that substrate 300 is a metal material (p.3, paragraph [0032]).

F) As to Claims 6, 7, 13 and 14:

I. Cheng et al., as modified by Wachtler et al. and Viswanathan et al. in conjunction with teaching of the above-cited *Accuratus* data sheets discloses that the thermally conductive substrate of the semiconductor package comprises an internal circuit that provides noise suppression, signal conditioning or impedance matching for the purpose of improving the performance of the semiconductor IC device of the package (see col.4: 49-col.5: 18 in Viswanathan et al.). It remains to be shown that Cheng et al., in view of Wachtler et al. and Viswanathan et al., also discloses that the internal circuit in the substrate comprises at least one of a capacitor and an inductor (Claims 6 and 13) and that the internal circuit and the bonding pads on the chip are electrically connected (Claims 7 and 14).

II. Viswanathan et al. further discloses that, in order to provide the above-cited circuit enhancements, the internal circuit 141 comprises at least one of a capacitor and an inductor (col.4: 49-57) and is electrically connected to the bonding pads on the chip

(the bonding pads 124 of semiconductor chip 130 are electrically connected to the internal circuit 141; see Figs. 1 and 3, and col.3: 20-25 and 39-46).

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the internal circuit of Cheng et al., as modified by Wachtler et al. and Viswanathan et al., with the inclusion of at least one of a capacitor and an inductor in order to form the particular noise suppression, signal conditioning or impedance matching circuit(s) required by the specific electronic application of the package, with the internal circuit being electrically connected to the chip bonding pads in order for the internal circuit of the substrate to perform the above-cited filtering and impedance operations for enhancing the performance of the chip and, thereby, the semiconductor package, as taught by Viswanathan et al.

G) As to Claims 15 and 23, Cheng et al. discloses: a substrate 300 having a first surface and at least one cavity 306 located on the first surface (Fig. 15); a chip 310 having an active surface 310a with a plurality of bonding pads 312 thereon and a backside surface 310b attached to the bottom of cavity 306 (Fig. 15; p.3, paragraph [0033]); and a build-up circuit structure on substrate 300 (Fig. 23; p.3: paragraphs [0033]-[0042]), the build-up circuit structure having at least one insulation layer 314a (Fig. 17; paragraph [0034]), at least one patterned circuit layer 320a (Fig. 19; p.3, paragraph [0037]) and a plurality of via openings 316 (Fig. 17), wherein the insulation layer 314a is located between the active surface 310a and the at least one patterned circuit layer 320a (Fig. 19), the via openings 316 corresponding to bonding pads 312 pass through the insulation layer (Fig. 17) {p.3, paragraph [0034]}, wherein the via

openings 316 are deposited with a conductive material 320 (Fig. 18; p.3: paragraph [0037]), the at least one patterned circuit layer 320a electrically connects with the bonding pads 312 through the conductive material 320 and a portion of the at least one patterned circuit layer 320a expands into a region outside the active surface of the chip (Fig. 19).

H) As to Claims 16 and 26, modified Cheng et al. further discloses a space between chip 310 and cavity 306 is filled by a portion of the material of insulation layer 314a (Figs. 16 and 17; p.3, lines 1-4 of paragraph [0034] and lines 1-5 of paragraph [0035]).

I) As to Claims 17 and 27, modified Cheng et al. further discloses a space between chip 310 and substrate 300 (i.e., the space between chip 310 and the wall of the substrate cavity 306) is filled by a portion of the material of insulation layer 314a (Figs. 16 and 17; p.3, lines 1-4 of paragraph [0034] and lines 1-5 of paragraph [0035]).

J) As to Claims 18, 24 and 25, modified Cheng et al. further discloses a plurality of solder ball pads on the at least one patterned circuit layer 326a, and a plurality of solder balls 330 attached to the solder ball pads, respectively (Fig. 24; p.3, paragraph [0040]).

K) As to Claim 19, modified Cheng et al. further discloses a passivation layer 328 disposed on the patterned circuit layer 326a, wherein passivation layer 328 has a plurality of openings 329 corresponding to the solder ball pads (Figs. 23 and 24; paragraph [0039]).

L) As to Claims 20 and 28, modified Cheng et al. further discloses that substrate 300 is a metal material (p.3, paragraph [0032]).

M) As to Claims 21, 22, 29 and 30:

I. Cheng et al., as modified by Wachtler et al. and Viswanathan et al. in conjunction with teaching of the above-cited *Accuratus* data sheets, discloses that the thermally conductive substrate of the semiconductor package comprises an internal circuit that provides noise suppression, signal conditioning or impedance matching for the purpose of improving the performance of the semiconductor IC device of the package (see col.4: 49-col.5: 18 in Viswanathan et al.). It remains to be shown that Cheng et al., in view of Wachtler et al. and Viswanathan et al., also discloses that the internal circuit in the substrate comprises at least one of a capacitor and an inductor (Claims 21 and 29) and that the internal circuit and the bonding pads on the chip are electrically connected (Claims 22 and 30).

II. Viswanathan et al. further discloses that, in order to provide the above-cited circuit enhancements, the internal circuit 141 comprises at least one of a capacitor and an inductor (col.4: 49-57) and is electrically connected to the bonding pads on the chip (the bonding pads 124 of semiconductor chip 130 are electrically connected to the internal circuit 141; see Figs. 1 and 3, and col.3: 20-25 and 39-46).

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the internal circuit of Cheng et al., as modified by Wachtler et al. and Viswanathan et al., with the inclusion of at least one of a capacitor and an inductor in order to form the particular noise suppression, signal

conditioning or impedance matching circuit(s) required by the specific electronic application of the package, with the internal circuit being electrically connected to the chip bonding pads in order for the internal circuit of the substrate to perform the above-cited filtering and impedance operations for enhancing the performance of the chip and, thereby, the semiconductor package, as taught by Viswanathan et al.

Response to Arguments

7. Applicant's arguments with respect to Claims 6, 13, 21 and 29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Since the Examiner indicated allowability for Claims 6-7, 13-14, 21-22 and 29-30 in the previous Office Action of August 25, 2004 and has now found new prior art with which to reject Claims 6-7, 13-14, 21-22 and 29-30 in the present Office Action, the present Office Action is therefore made NON-FINAL.

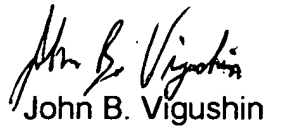
9. In the previous Office Action of August 25, 2004, the Examiner cited Sakamoto et al. (US Patent Application Publication 2004/0014317 A1) as prior art. The Examiner now recognizes that he was in error in doing so since the PCT filing date of April 25, 2001 is not the qualifying date for prior art because it is not a publishing date. In the instant case, only the publishing date of the US Patent Application Publication 2004/0014317 A1 can be used to determine the prior art status. That publication date is January 22, 2004, which is later than the filing date of Applicant's instant Application.

Accordingly, the description of the disclosure of US 2004/0014317 A1 remains of record in the instant Application only as a citation of "related" art of interest but not qualifying as prior art against the claims in the instant Application. The Examiner apologizes for the error.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
February 21, 2005